

On the MAGIC-II DAQ for PET-TOF

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Our information sources

- **Student thesis**

- *"Ultra-fast sampling and readout for the MAGIC-II telescope Data Acquisition System", Massimiliano Bitossi at Universita di Pisa, 2009.*
 - due to non-disclosure agreements, chapters on MAGIC-II upgrade to DRS4 are missing

- **PSI Docs on DRS**

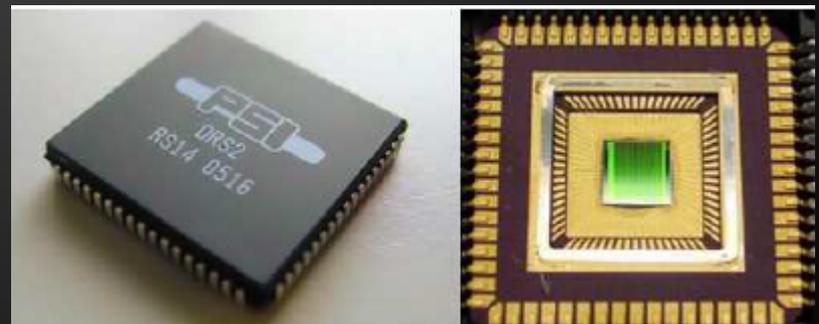
- <http://drs.web.psi.ch/docs/>

MAGIC Telescope Specs

- Interested in recording fast signals
 - 2 ns FWHM
 - signals travel 80 m optically
- Trigger rate of few kHz
- Make use of Switch Capacitor Array (SCA) used as a circular buffer for fast sampling
 - stopped by trigger
 - signal current of ~ 1 mA needed
 - readout must occur < 1 ms after trigger

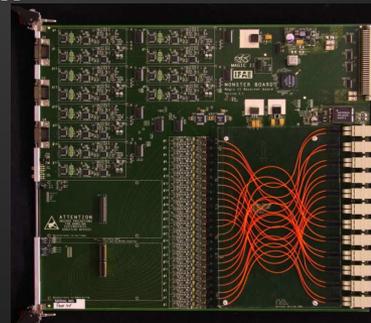
MAGIC-II DAQ Components

- **DRS2 - Domino Ring Sampler version 2**
 - 0.25 micron process in 2004, rad-hard
 - 0.5 to 4.5 Gbps (used at 2 Gbps);
 - 40ps jitter at 2.5 GHz
 - >500 MHz bandwidth
 - 10 channels with 1024 samples
- **DRS2 Mezzanine card**
 - 2 DRS2 chips ∴ 20 analog channels
 - Digitizes at 40 MHz, 12-bits



MAGIC-II DAQ Components Cont.

- **PULSAR board**
 - 4 DRS2 Mezzanine cards ∴ 80 analog channels
 - 3 FPGAs (Altera Apex 20K; 500 I/O; \$970 ea.)
 - communicate through VME backplane, 9U
 - Clock and trigger at front panel
 - 320 MBps
- **MONSTER board**
 - 24 channels
 - converts optical to electrical
 - generates trigger
 - handles calibration



MAGIC-II DAQ Components Cont.

- Full System
 - 14 analog PULSARs
 - 1 dedicated trigger PULSAR
 - 1 dedicated busy PULSAR
 - 2 9U VME crates
 - 1132 channels

More on DRS2

- Input clock is 1/1024 of sampling frequency
 - Critical timing needed for digital control signals to run chip at high speeds (on order 100 ps)
- Sampling by 200 fF caps
- Large variations from cell to cell, temperature and power supply dependent
 - Requires "extended" calibration "regularly"
- 2% "ghosting" at 2 GHz
- Systematic charge leakage error for readout
- 256 us dead time "required"
- \$70/channel

DRS4

- 9 channels
 - read out in parallel
 - read out only region of interest
 - can cascade channels and/or daisy-chain chips
 - $<100\text{ns}$ dead time achievable, but <8 channels
- designed to self trigger
- clock out sampling cells at 33 MHz (30 nsps)
 - 30 μs for 1024 samples
- Less systematic charge leakage, 150 fF caps
- Simpler controls
- Jumping through hoops gives <10 ps jitter
- \$10/ch

Example DRS4 Implementation 1

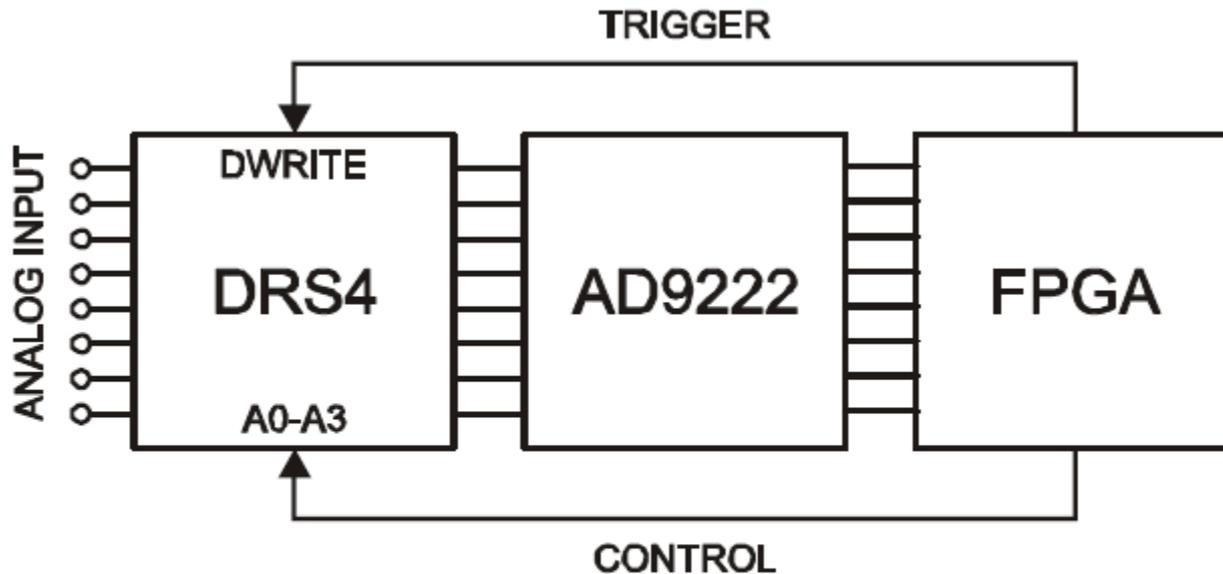


Figure 8. Simultaneous Waveform Digitizing and Triggering using the same ADC

- AD9222 is \$50
- Could use comparator ASIC for trigger (AD8564 ~\$1/ch)

Example DRS4 Implementation 2

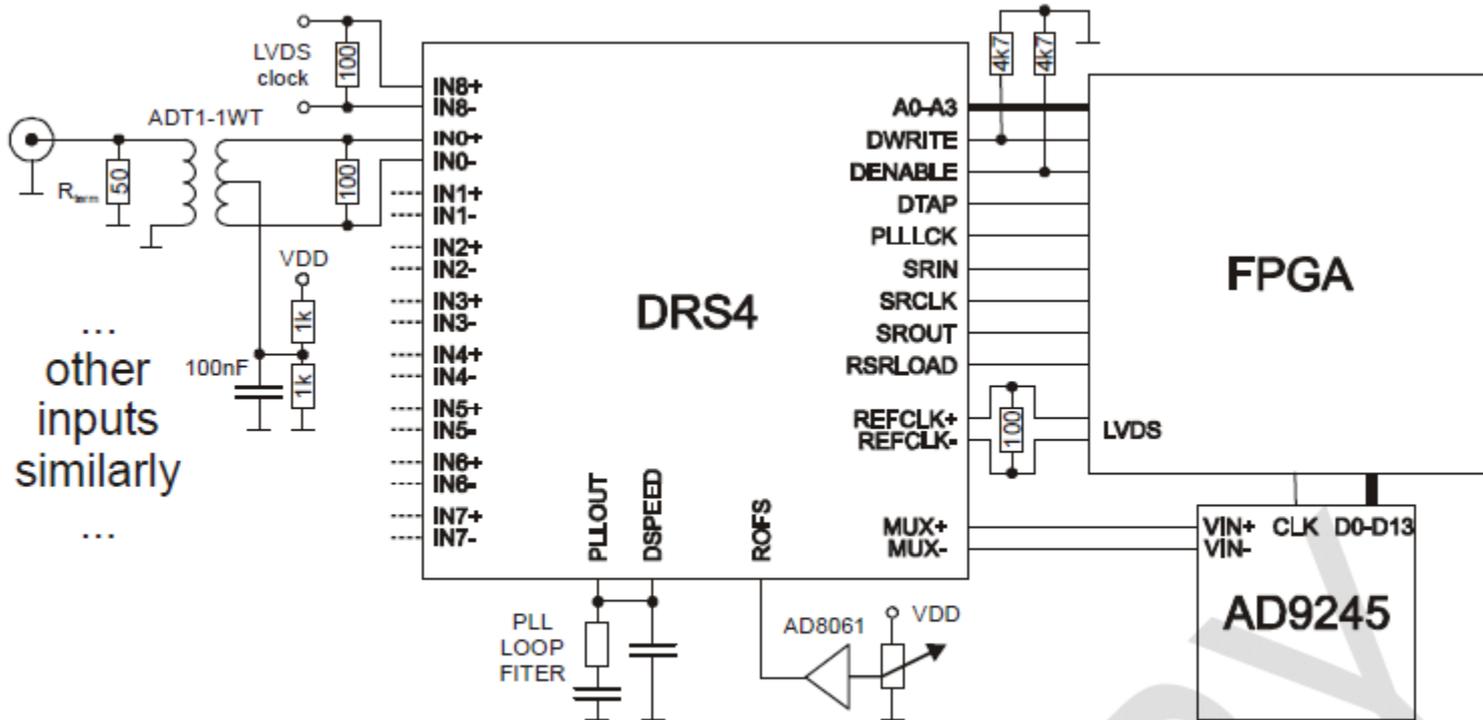


Figure 17. Typical Mode of Operation

- AD9245 is \$20
- Could use comparator ASIC for trigger (AD8564 ~\$1/ch)