PET-TOF Electronics

Preliminary Proposal

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1. Introduction

We are proposing architecture of a Time-of-Flight (TOF) Positron Emission Tomography (PET) electronics that will let to achieve high overall system efficiency (approximately 200ps FWHM precision at very high trigger rate of 400 KHz) thus allowing reduction in radiation intake by a patient. The proposal concerns mainly front end or "helmet" electronics and does not discuss aspects of the DAQ. Together the proposed architecture and a preliminary construction of the "helmet" electronics are designed for simplicity and manufacturability hence laying foundation for reduction in system's cost in the future.

2. System Description

The "helmet" electronics performs several major functions which include:

- Amplification and filtering of initial "raw" signals coming from an array of Silicon Photomultipliers (SiPM);
- Storing amplified waveforms in an analog memory until trigger decision is reached;
- Digitization of analog information residing within a "region of interest" (ROI) in the analog memory and shipping digital data to a buffer memory when a trigger is accepted;
- Synchronization of the shipped data with a common clock to keep precise spatial information about the source of the event
- Implementation of the Ethernet protocols for shipping packets of data from the buffer memory to a Data Acquisition System (DAQ).

Mechanically, the "helmet" electronics is built as a combination of eighteen identical Signal Processing Units, each of which consists of two Preamplifier Boards (see Figure 1) and a single Signal Processing Board which in turn is a sandwich of three PC boards (see Figure 2):

a) two daughter boards:
   - Amplifier & Trigger Board and
   - DRS Board

b) and the mother board called
   - FPGA and Clock Board.

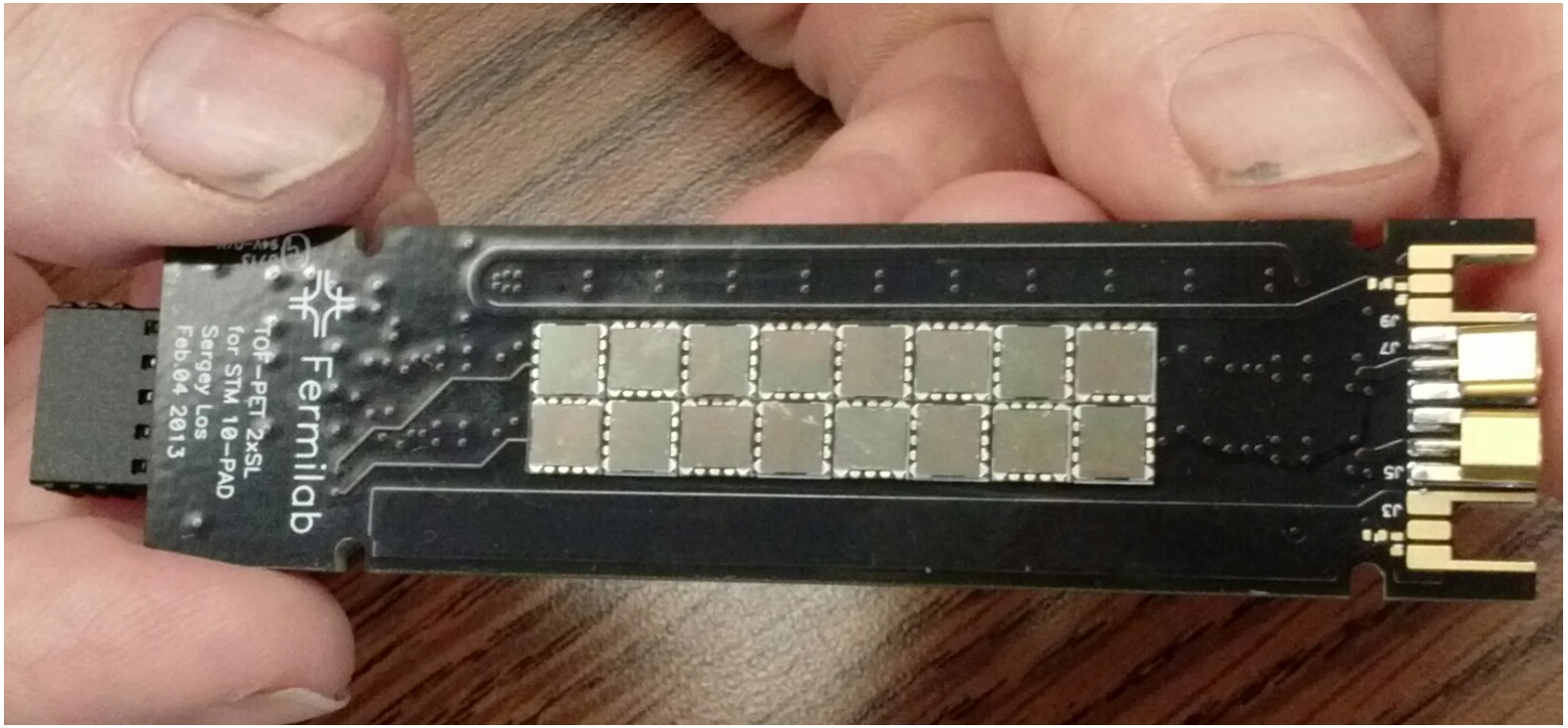

Fig. 1 Preamplifier Board (by Sergey Los)

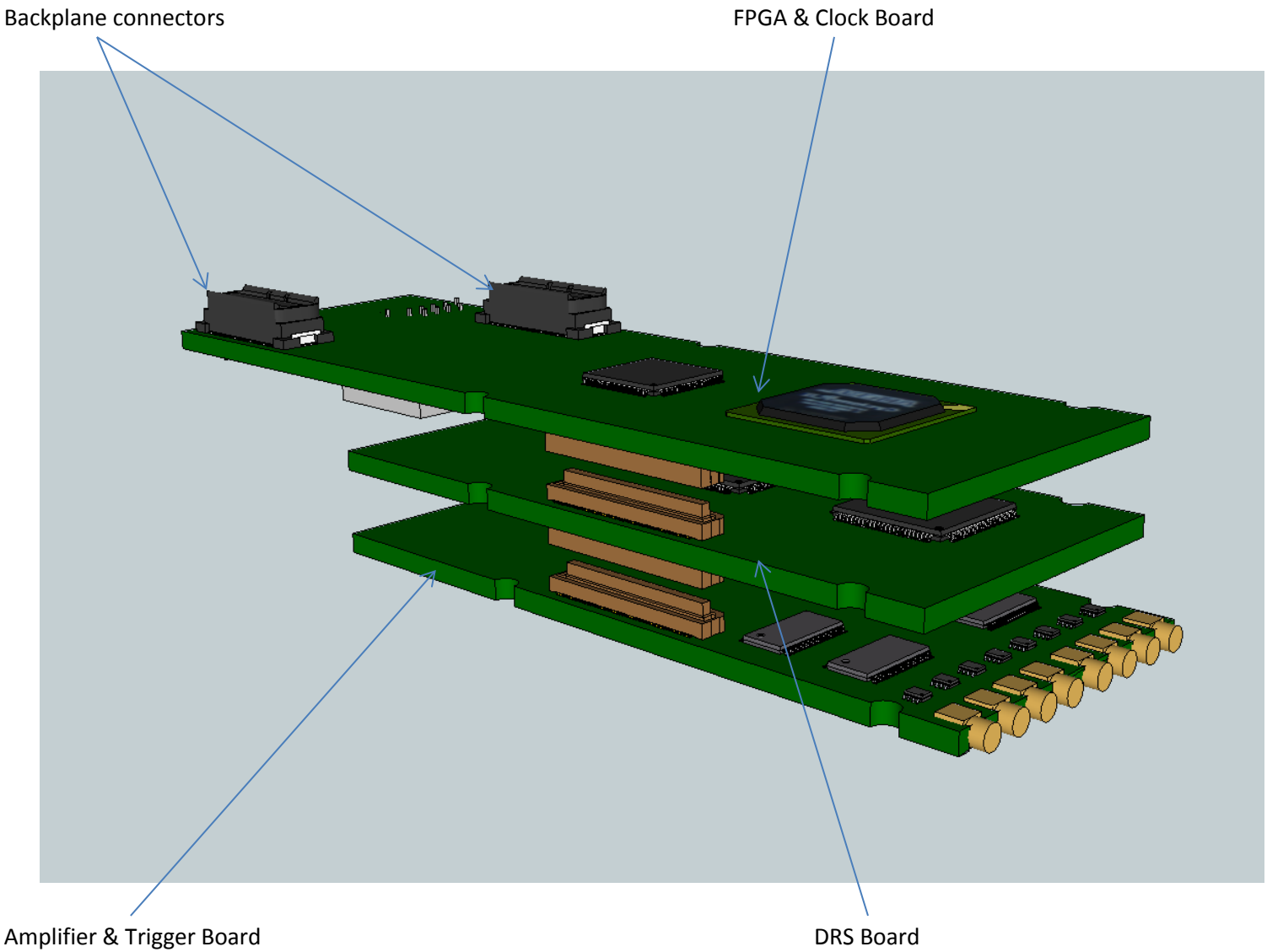

Fig. 2 Signal Processing Board (by Mark Kozlovsky and Paul Rubinov)

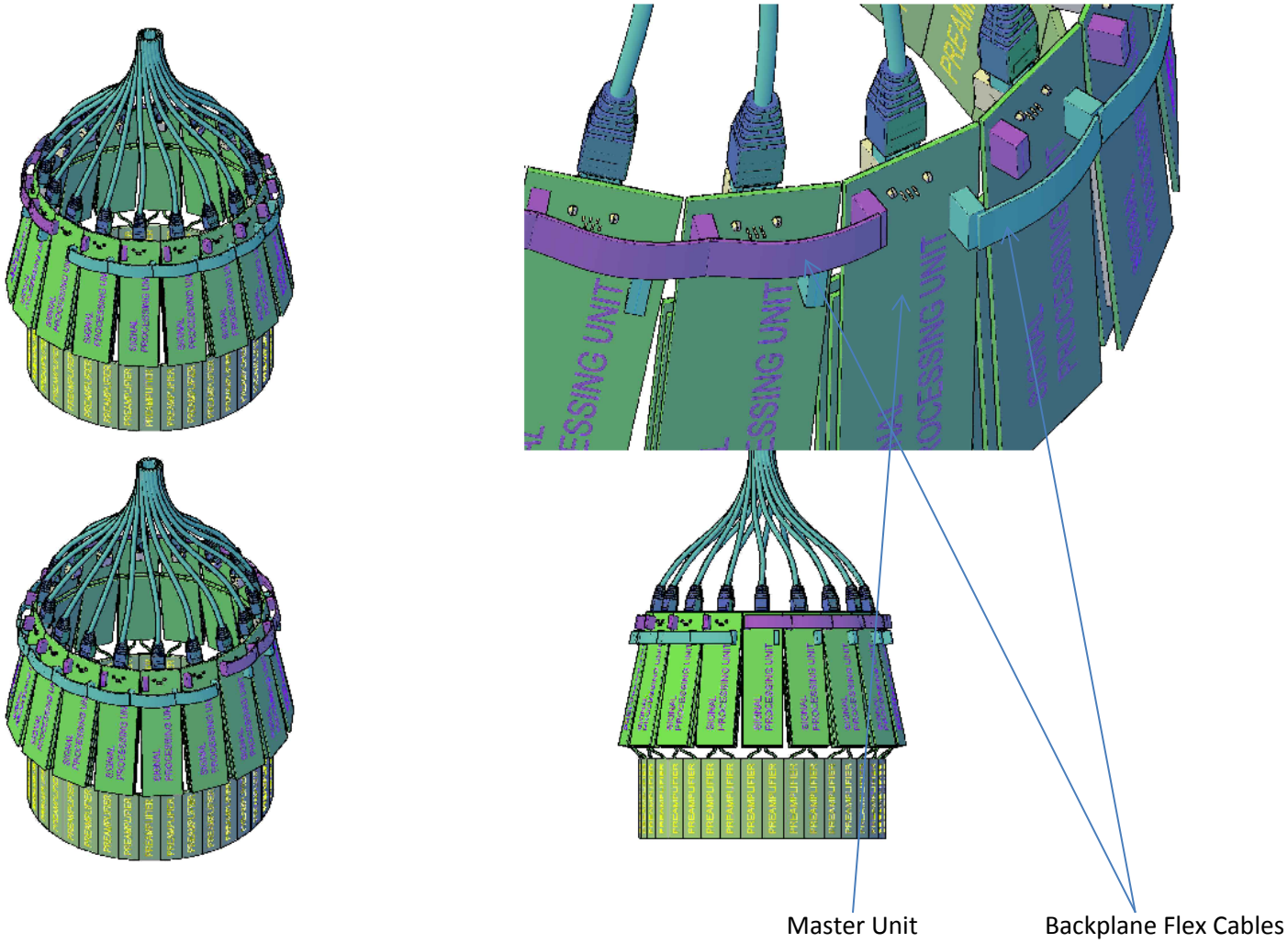

Fig. 3 Construction of the “helmet electronics” (by Mark Kozlovsky and Dave Huffman)

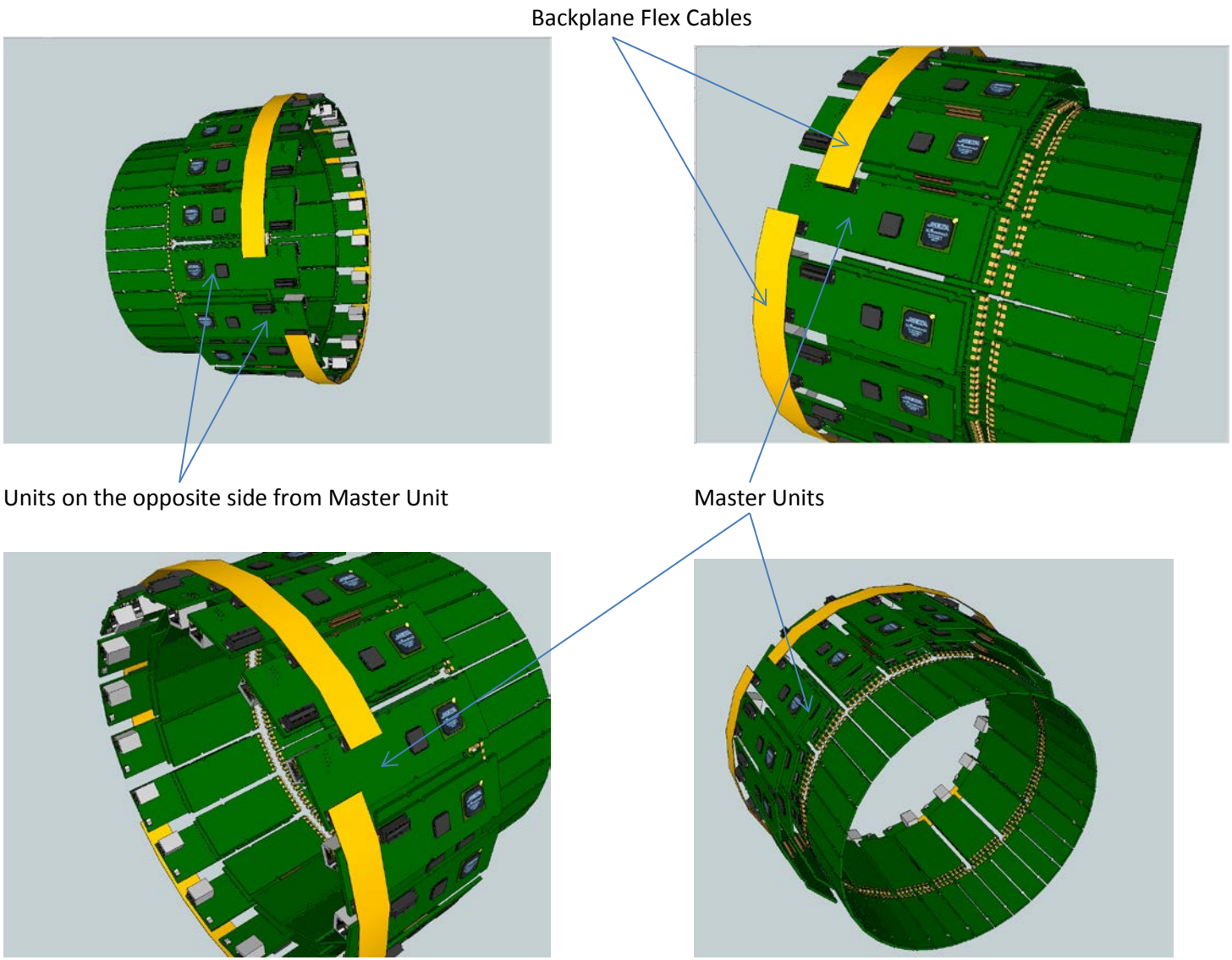

Fig. 4 Various views of the “helmet” electronics’ construction (by Mark Kozlovsky and Paul Rubinov)

All the Signal Processing Units are placed in a “helmet” like structure, cartoon renderings of which are shown in Figures 3 and 4. Among themselves, the units are connected via two flat flex cables holding multiple connectors that perform the role of two backplanes.

The backplanes link all units into a master-slave configuration where only one unit serves as the master for both trigger and clock distribution. The master unit is distinguished by having both backplane connectors engaged (this is also shown in Figures 3 and 4). Although all units are identical, engaging both backplane connectors activates the part of the unit’s internal electronic circuitry responsible for collecting local trigger signals from all other units and making and distributing a trigger decision. It is also responsible for generating and distributing clock signals common to all the units.

Utilizing backplanes and master-slave configuration allows all the connections on the backplanes to be peer-to-peer differential pairs, which allows for proper line terminations and noise reduction. The latter permits almost simultaneous distribution of the trigger signal from the master to all other units and low jitter clock distribution.

All units transfer data to DAQ via individual Ethernet cables. That significantly reduces the number of connections coming to the “helmet” electronics. It also allows us to eliminate connections needed for power distribution, as power for each unit can be derived directly from Ethernet via the method known as “power-over-the-Ethernet”. Up to 20W power can be delivered to each unit without additional wires using this method.

3. Signal Processing Unit

The Signal Processing Unit (SPU) is at the heart of proposed electronics. Its circuit block diagram is shown in Figure 5. The unit is built around a set of the following components:

a) Mini-Circuits GALI-S66+ - a wideband amplifier used in the preamplifiers;
b) Analog Devices ADA4960 – ultra high speed differential ADC driver used to build differential amplifiers;
c) Analog Devices AD8003 – triple high bandwidth amplifier, ADCMP600 – rail-to-rail very fast comparator, and Maxim MAAX5725 octal-channel DAC used to build trigger circuitry;
d) PSI DRS4 – 9-channel, 5 GSPS switched capacitor array used for sampling and storage of raw analog information coming out of SiPMs;
e) Analog Devices AD9222 – octal, 12-bit, 65 MSPS ADC designed to work directly with the DRS4 and Texas Instrument ADS4122 – single 12-bit 65 MSPS ADC both used to digitize analog and timing signals coming out of DRS4 ;
f) Maxim MAX1932 – digitally controlled precision bias supply used to bias SiPMs;
g) Xilinx SPARTAN-6LXT Series of FPGAs (XC6SLX45T), Micrel KSZ9021RN Gigabit Ethernet Transceiver, Micron MT47H64M16 – 8 Meg × 16 × 8 banks DDR2 SDRAM, Future Technology FT232HL – high speed USB controller all used to build digital part of the unit’s control, processing, and interface circuitry on the FPGA & Clock Board;

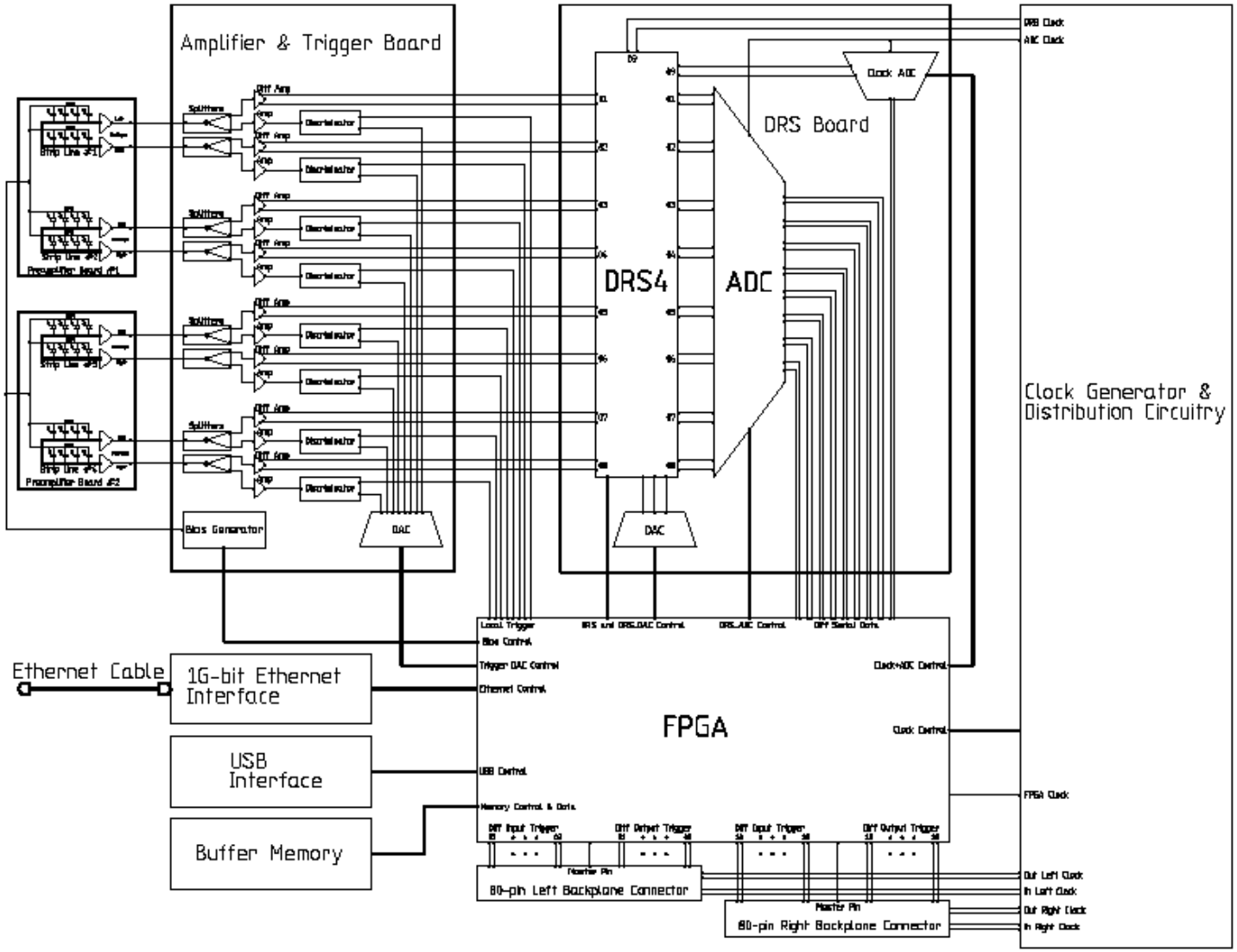

Fig. 5 Signal Processing Unit Block Diagram (by Mark Kozlovsky)

a) Texas Instrument LMK04906 – ultra low noise clock jitter cleaner/multiplier with six programmable outputs used to build clock and clock distribution circuitry.

Initial raw signals formed by SiPMs connected to the strip lines are amplified and filtered by high frequency output amplifiers residing on the Preamplifier Boards. Those amplifiers provide an approximate gain of 10. In order to fully utilize the whole dynamic range of DRS and digitizing ADC these signals are further amplified by gain of 6 in the Amplifier & Trigger Board and transformed from single ended to differential in order to correspond to the input requirements of the DRS4. The overall gain of 60 together with 12-bit resolution of the ADC and dynamic range of DRS4 at 1V bring the sensitivity of our instrumentation to approximately 400 electrons (input referred) per cell at full sampling rate of 5 GSPS.

Differential analog waveforms are stored into the DRS4 chip until trigger signal is found. The latter is formed by the FPGA inside the master unit and instantaneously distributed to all the other units. This is done by analyzing local triggers which are generated inside and shipped to the master from all the slave units. When trigger is issued, all the units stop acquiring analog waveforms and start transferring the charge stored inside DRS4"region-of-interest" into the digitizer (ADC) and then via FPGA to the buffer memory.

In our design trigger path is completely separated from the signal path. To achieve this, the input analog waveforms are split into two identical waveforms right at the beginning and then are similarly amplified. The trigger waveform goes to the discriminator where it is compared with a individually controlled predefined level. When the threshold is exceeded, the FPGA forms a local trigger and issues it to the master unit.

Buffer memory is to undo randomization of the data for readout by the DAQ via Ethernet. Because a common clock is also a part of read data, the synchronization of data with the clock is easily realized by the DAQ thus allowing for precise timing of the signals.

Right and left backplanes, which are essentially custom high density flexible flat printed circuits, provide peer-to-peer differential connections between the units. The trigger connections are star distributed from the master unit while the clock connections on each cable are sequential going from unit to unit and having both input and output points of entrance. The clock transfer between these points is made inside the LMK04906 chip. As the internal jitter of this chip does not exceed 130 femtoseconds, the entire jitter across the cable will not be bigger than 2.34 picoseconds which create only ~1.2% uncertainty in clock edge positioning for 5GHz clock.

4. Summary

The proposed architecture and design of the PET-TOF electronics allows the project to meet all of the design goals for this type of instruments, i.e.

- High system efficiency to reduce patient intake of radioactive materials (~200ps FWHM precision at very high trigger rate of ~400KHz)
- High system sensitivity of less than ~400 electrons per cell at the input at full sampling rate of 5 GSPS
- High system precision derived from only 1.2% uncertainty in clock positioning for 5GHz clock
- Low latency, low jitter peer-to-peer distribution of trigger signals
- Ultralow jitter clock distribution
- Simple construction as it uses a minimal quantity of cables to assemble the system and connect it to the DAQ
- No additional power distribution connections as power is delivered over the Ethernet
- Lower engineering, manufacturing, maintenance, and debugging coasts as all the Signal Processing Units are identical